ABSTRACT

The SRAM-compatible memory device includes a first pair of bit lines for transferring data fetched from/written in a DRAM cell in a first memory block, a second pair of bit lines for transferring data fetched from/written in a DRAM cell in a second memory block. Further, the SRAM-compatible memory device includes the first sense amplifier for amplifying and latching data in the first pair of bit lines, a second sense amplifier for amplifying and latching data in the second pair of bit lines, a third sense amplifier for amplifying and latching data transferred whereto, a first switching unit for controlling an electrical connection between the first pair of bit lines and the third sense amplifier, and a second switching unit for controlling an electrical connection between the second pair of bit lines and the third sense amplifier.